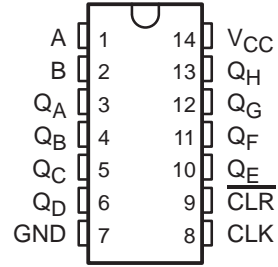


# SN74HC164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear

S74HC16N PACKAGE  
(TOP VIEW)



### description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear ( $\overline{\text{CLR}}$ ) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

The SN74HC164 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

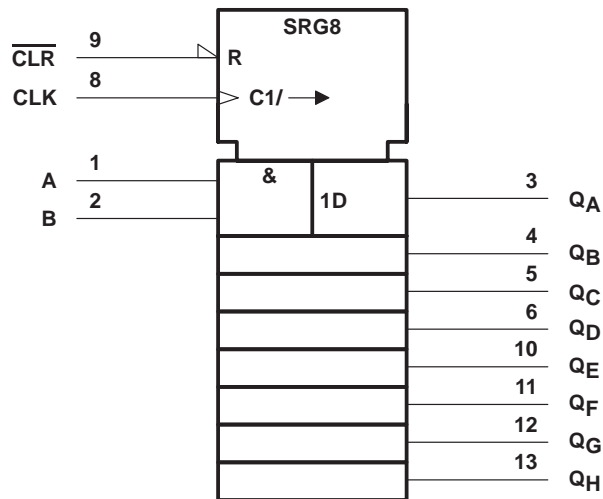
INPUTS				OUTPUTS		
$\overline{\text{CLR}}$	CLK	A	B	$Q_A$	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	$\uparrow$	H	H	H	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	L	X	L	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	X	L	L	$Q_{An}$	$Q_{Gn}$

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{H0}$  = the level of  $Q_A$ ,  $Q_B$ , or  $Q_H$ , respectively, before the indicated steady-state input conditions were established

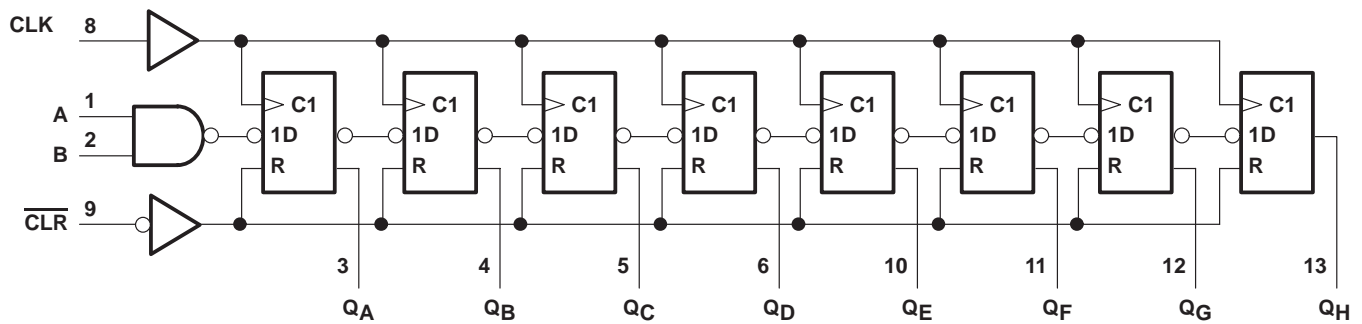
$Q_{An}$ ,  $Q_{Gn}$  = the level of  $Q_A$  or  $Q_G$  before the most recent  $\uparrow$  transition of CLK: indicates a 1-bit shift

SN74HC164  
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

logic symbol†



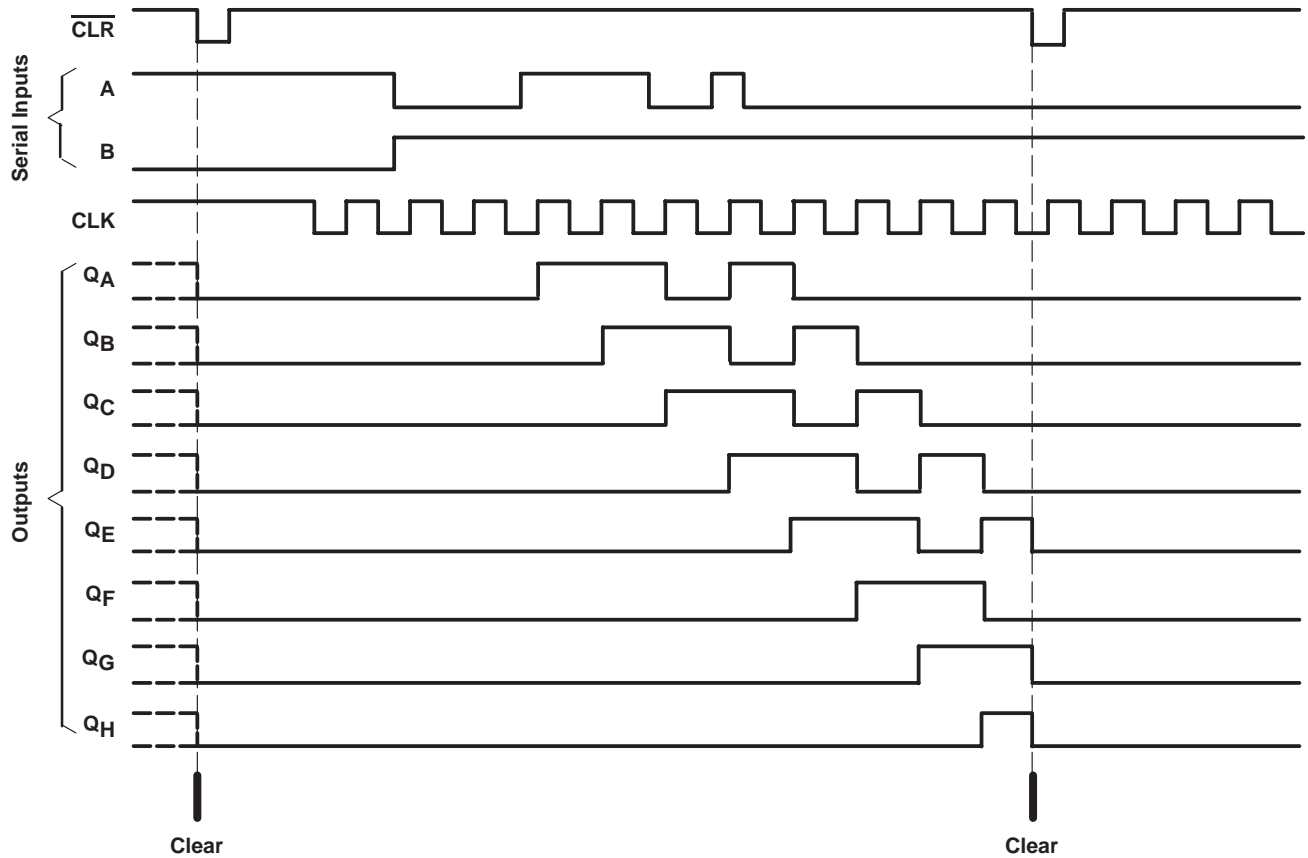
logic diagram (positive logic)



Pin numbers shown are for the N packages.

**NOTE: Port A and Port B can not connect captance**

typical clear, shift, and clear sequence



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): N package .....	78°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

# SN74HC164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

### recommended operating conditions

		S74HC164			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0	0.5	V
		V <sub>CC</sub> = 4.5 V	0	1.35	
		V <sub>CC</sub> = 6 V	0	1.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		V
t <sub>t</sub> <sup>†</sup>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6 V	0	400	
T <sub>A</sub>	Operating free-air temperature	-40	85		°C

† If this device is used in the threshold region (from V<sub>ILmax</sub> = 0.5 V to V<sub>IHmin</sub> = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			S74HC164		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9		V
			4.5 V	4.4	4.499	4.4		
			6 V	5.9	5.999	5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.84		
			6 V	5.48	5.8	5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.002		0.1	0.1	V
			4.5 V	0.001		0.1	0.1	
			6 V	0.001		0.1	0.1	
		I <sub>OL</sub> = 4 mA	4.5 V	0.17		0.26	0.33	
			6 V	0.15		0.26	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1		±100	±1000	nA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8	80	μA	
C <sub>i</sub>		2 V to 6 V	3		10	10	pF	

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## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		S74HC164		
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	0	6	0	5	MHz
		4.5 V	0	31	0	25	
		6 V	0	36	0	28	
t <sub>w</sub>	Pulse duration	$\overline{\text{CLR}}$ low	2 V	100	125		ns
			4.5 V	20	25		
			6 V	17	21		
	CLK high or low	2 V	80	100			
		4.5 V	16	20			
		6 V	14	18			
t <sub>su</sub>	Data	Data	2 V	100	125		ns
			4.5 V	20	25		
			6 V	17	21		
	$\overline{\text{CLR}}$ inactive	2 V	100	125			
		4.5 V	20	25			
		6 V	17	21			
t <sub>h</sub>	Hold time, data after CLK↑		2 V	5	5		ns
			4.5 V	5	5		
			6 V	5	5		

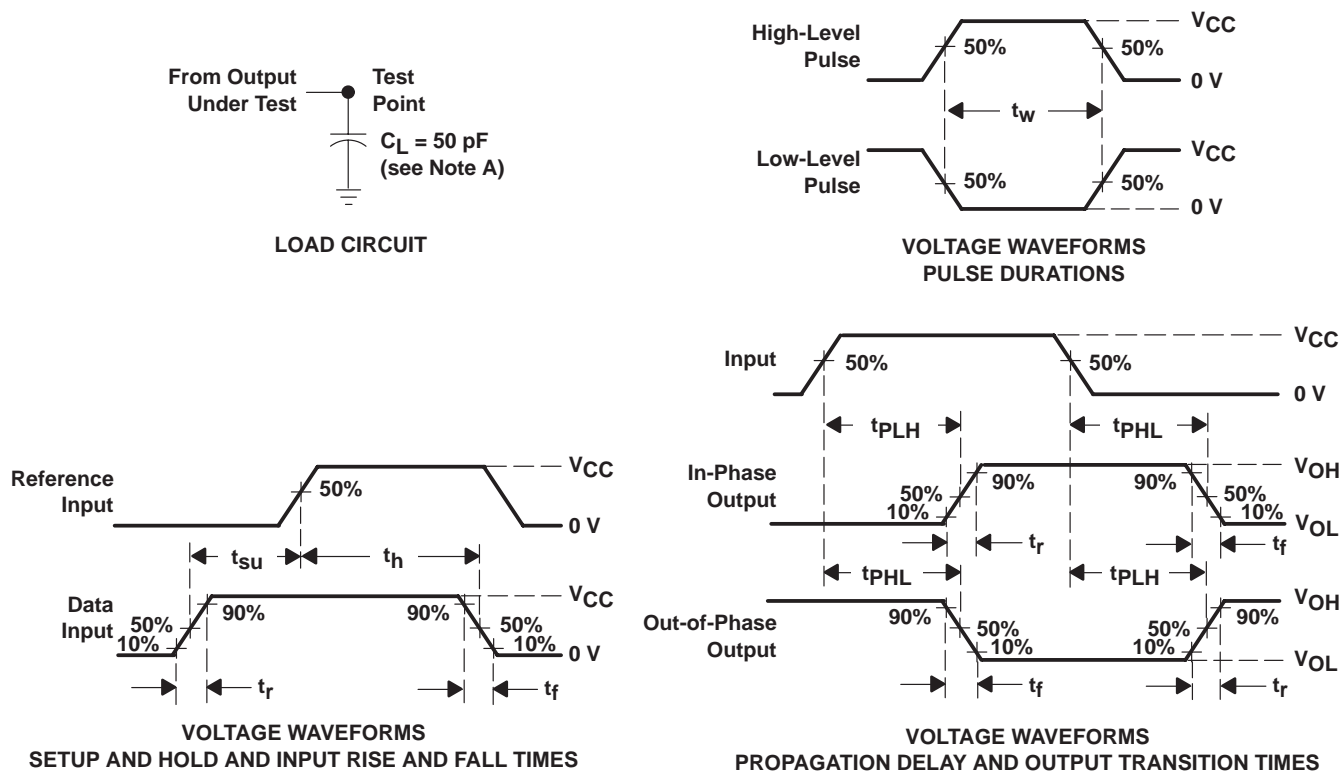
switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			S74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	10		5	MHz	
			4.5 V	31	54		25		
			6 V	36	62		28		
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Any Q	2 V		140	205	255	ns	
			4.5 V		28	41	51		
			6 V		24	35	46		
t <sub>pd</sub>	CLK	Any Q	2 V		115	175	220	ns	
			4.5 V		23	35	44		
			6 V		20	30	38		
t <sub>t</sub>			2 V		38	75	95	ns	
			4.5 V		8	15	19		
			6 V		6	13	16		

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	135 pF

**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**